

DOCKET NO: 282371US40PCT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :
TAKASHI KARIYA, ET AL. : EXAMINER: NEIL ABRAMS
SERIAL NO: 10/564,200 :
FILED: JANUARY 11, 2006 : GROUP ART UNIT: 2839
FOR: INTERPOSER AND MULTILAYER :
PRINTED WIRING BOARD :

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is an appeal from a final Office Action mailed January 2, 2009. A Notice of Appeal was timely filed on July 2, 2009.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is IBIDEN CO., LTD., 1, Kandacho 2-chome, Ogaki-shi, Gifu, Japan 503-8604.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative and the assignees are aware of no appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-3 and 5-22 are pending, stand rejected and are herein appealed. Claim 4 is canceled.

IV. STATUS OF THE AMENDMENTS

No amendments have been made after final action in this case. The attached Appendix VIII reflects Claims 1-3 and 5-22 as presently pending on appeal.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 1 recites an interposer configured to be located between a package substrate made of resin and an IC chip.¹ The interposer includes an insulating base material.² A Young's modulus of the insulation base material is 55 to 400 GPa, and a thickness of said insulation base material is 0.05 to 1.5 times the thickness of the package substrate.³ A plurality of through holes are provided through the insulating base material.⁴ Each of the plurality of through holes has a diameter of 125 μm or less and has formed therein a through hole conductor for connecting the package substrate with the IC chip.⁵ The plurality of through holes in the insulating base material are arranged in the form of a grid.⁶ Similarly, independent Claim 11 recited an interposer configured to be located between a package substrate made of resin and an IC chip.⁷ The interposer includes an insulating base material.⁸ A young's modulus of the insulation base mater is 55 to 440 GPa and a thickness

¹ See Fig. 3 and page 14, lines 18-22 of the specification.

² See Fig. 2 and page 14, lines 22-27 of the specification.

³ See page 4, lines 12-22 of the specification.

⁴ See Fig. 3 and page 14, lines 22-25 of the specification.

⁵ See Fig. 3 and page 8, line 31 - page 9, line 5 of the specification.

⁶ See page 9, lines 5-7 of the specification.

⁷ See Fig. 3 and page 14, lines 18-22 of the specification.

⁸ See Fig. 2 and page 14, lines 22-27 of the specification.

of said insulation base material is 0.05 to 1.5 times the thickness of the package substrate.⁹ A plurality of through holes are provided through the insulating base material.¹⁰ Each of said plurality of through holes has a diameter of 125 μm or less and has formed therein a through hole conductor for connecting said package substrate with the IC chip.¹¹ The plurality of through holes in the insulating base material are arranged in the form of a staggered arrangement.¹²

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3 and 5-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,836,011 to Azuma, in view of U.S. Patent 5,325,265 to Turlik et al., U.S. Patent 6,335,210 to Farooq et al., JP 11-054884 to Ikeda, U.S. 6,516,513 to Milkovich et al., U.S. 6,452,807 to Berrett and JP 59-000996 (hereinafter “JP ‘996”). This ground of rejection is presented for review in this appeal.

VII. ARGUMENTS

A. **None of the cited references disclose the claimed thickness of the insulating base.**

As noted above and shown in the claims appendix, independent Claims 1 and 11 recite that a

Young’s modulus of insulation base material is 55 to 440 GPa and a thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate.

The final Office Action acknowledges that none of Azuma, Turlik et al., Farooq et al., Ikeda, Milkovich et al., Berrett and JP ‘996 disclose that the “thickness of the insulating base

⁹ See page 4, lines 12-22 of the specification.

¹⁰ See Fig. 3 and page 14, lines 22-25 of the specification.

¹¹ See Fig. 3 and page 8, line 31 - page 9, line 5 of the specification.

¹² See page 9, lines 5-7 of the specification.

material is 0.05 to 1.5 times the thickness of the package substrate.” The Office Action concludes that this feature is depicted in the drawings or obvious to one skilled in the art due to design and manufacturing considerations.

However, none of the cited references discuss anything about thickness values of the interposer in relation to the package substrate, and none of the cited references disclose scaled drawings by which one could measure and calculate the thickness range based solely on the drawings. Appellants submit that the final Office Action provides only general assertions that the thickness range “is too broad” or falls within “normal production” techniques, which cannot support a finding that the cited references disclose that the “thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate,” as required by Claims 1 and 11. Stated differently, the Final Office Action has not presented a *prima facie* case that the above feature is taught or suggested by the cited references.

B. It would not be obvious for one of ordinary skill in the art to combine a teaching of the claimed thickness feature with a teaching of the claimed Young’s modulus feature.

Even assuming for purposes of this Appeal that the claimed thickness range is found in the prior art, one of ordinary skill in the art would not combine the claimed interposer thickness range with the claimed Young’s modulus range to arrive at Appellants’ claimed invention. As discussed in the Background section of Appellants’ specification, high frequency IC chips are typically made of a brittle porous material that is prone to cracking under thermal stress. Thus, stress defects in the IC chip occur during loading of the substrate with the IC.¹³ Appellants’ invention is directed to addressing this problem. The present inventors analyzed thermal stress during loading of the IC onto the substrate under various conditions and discovered a particular advantage to combining the claimed Young’s modulus

¹³ See specification at paragraph linking pages 1 and 2.

and thickness.¹⁴ That is, the inventors discovered that the combined features of the claimed Young's modulus and the claimed thickness range provide an improved configuration that suppresses deformation of the insulation base material and crevice or breaking in the resin layer of the IC. None of the seven references combined for rejecting Claims 1 and 11 disclose any importance of the thickness relationship of an interposer to a package substrate, let alone this relationship in combination with the claimed thickness range. In view of this, Appellants submit that combination of these features is impermissible hindsight reasoning based on Appellants' disclosure.

Thus, the cited references do not disclose or render obvious the feature of a Young's modulus of insulation base material is 55 to 440 GPa *and* a thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate. This alone provides reason for allowance of Claims 1 and 11.

C. None of the cited references disclose the claimed through hole diameter.

Appellants' Claims 1 and 11 also recite,

each of the plurality of through holes having a diameter of 125 μ m or less and having formed therein a through hole conductor for connecting said package substrate with the IC chip.

As discussed in Appellants' specification, when the diameter of the through hole is 125 μ m or less, the amount of heat generation increases in the through holes because conductor resistance increases. The claimed invention is directed to this particular situation in which a small diameter through hole (125 μ m or less) generates excessive heat.

None of the references in the cited combination of Azuma, Turlik et al., Farooq et al., Ikeda, Milkovich et al., Berrett and JP '996 (and nor does Chang and Uchikawa et al.) disclose the feature of the plurality of through holes having a diameter of 125 μ m or less.

¹⁴ See specification at page 7, line 14 - page 8, line 3.

That is, none of the cited references disclose the claimed feature which causes the reliability problems discussed in the specification and addressed by the claimed invention. In this regard, Appellants note that the outstanding Office Action does not cite any references as teaching this feature, but rather takes the position that the limitation of a diameter of 125 μm or less “is seen to be a matter of typical engineering design.” However, the Office Action does not provide a plausible reason why one of ordinary skill in the art would limit a design of the interposer to this diameter size through hole. Thus, through holes having a diameter of 125 μm or less provides another patentable distinction of the claimed invention over the cited references.

D. None of the cited references disclose through holes in the claimed grid or staggered arrangement.

The claimed through hole size is not claimed in isolation, but rather in combination with the inventive solution that mitigates problems that arise from the small diameter size feature. That is, if one skilled in the art chose to design an interposer having through holes with the recited small diameter, then the resulting interposer would have the problems that Appellants specification discusses in the Background. But Appellants’ Claims 1 and 11 also recite,

Claim 1... wherein the plurality of through holes in the insulating base material are arranged *in the form of a grid*.

Claim 11... wherein the plurality of through holes in the insulating base material are arranged *in the form of a staggered arrangement*.

As noted above, when the diameter of the through hole is small, the amount of heat generation increases in the through holes because conductor resistance increases. Where the through holes are disposed in the form of the grid (as in Claim 1) or in the staggered fashion (as in Claim 11), “the temperature distribution of the interposer at the time of usage becomes uniform so that no stress concentrates on any specific location thereby the insulation layer of

the IC chip being not damaged. Further, the physical property (thermal expansion coefficient, Young's modulus and the like) of the insulation base material just below the IC chip becomes uniform because the through holes are formed uniformly."¹⁵ None of the cited references disclose this additional feature of the through holes being in a grid or staggered arrangement. This provides an additional basis for patentability of independent Claims 1 and 11 over the cited references.

E. None of the cited references disclose the feature of Claims 8 and 17.

Nevertheless, dependent Claims 8 and 17 recite that the diameter of an opening in at least an end face of the through hole is equal to or larger than the diameter of the hole in the center of the through hole. As discussed in Appellants' specification, this feature provides advantages of reducing heat and thermal stress in the area of the through hole.¹⁶ None of the cited references disclose this feature, and thus, the above dependent claims provide additional bases for patentability over the cited references.

F. None of the cited references disclose the features of Claims 20 and 25

Further, Claims 20 and 21 specify that the a set of said plurality of through holes corresponding to either a power source electrode or ground electrode terminal of the IC chip are arranged in said grid to effect substantially uniform temperature of the interposer. Similarly, Claim 22 recites that the plurality of through holes are arranged at substantially equal distance from each other. As discussed in Appellant's specification, these features further reduce thermal stress on the interposer.¹⁷ None of the cited references disclose this feature, and thus, the above dependent claims provide additional bases for patentability over the cited references.

¹⁵ Appellants' specification at paragraph 23.

¹⁶ Appellants' specification at paragraph 24.

¹⁷ Appellants' specification at paragraph 23.

CONCLUSION

For the reasons discussed above, all pending claims patentably define over the cited references. Therefore, the rejection should be reversed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

A handwritten signature in dark ink, appearing to read 'E. Garlepp', is written over a horizontal line.

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VIII. CLAIMS APPENDIX

Claim 1: An interposer configured to be located between a package substrate made of resin and an IC chip, the interposer comprising:

an insulating base material, wherein a Young's modulus of the insulation base material is 55 to 440 GPa and a thickness of said insulation base material is 0.05 to 1.5 times the thickness of the package substrate; and

a plurality of through holes provided through the insulating base material, at each of said plurality of through holes having a diameter of 125 μm or less and having formed therein a through hole conductor for connecting said package substrate with the IC chip,

wherein the plurality of through holes in the insulating base material are arranged in the form of a grid.

Claim 2: The interposer according to Claim 1, wherein the thickness of said insulation base material is at least 0.08 times the thickness of core of the package substrate.

Claim 3: The interposer according to Claim 1, wherein the size of said insulation base material is equal to or larger than a projection area of an electronic component loaded on the interposer, and equal to or less than a projection area of the package substrate.

Claim 5: The interposer according to Claim 1, wherein said package substrate is a multilayer printed wiring board.

Claim 6: The interposer according to Claim 1, wherein said through hole conductor is made of metal plating.

Claim 7: The interposer according to Claim 1, wherein said through hole conductor is made of metallic paste.

Claim 8: The interposer according to Claim 1, wherein as regards the sectional shape of the through hole in the insulation base material, the diameter of an opening in at least an end face of the through hole is equal to or larger than the diameter of the hole in the center of the through hole.

Claim 9: A multilayer printed wiring board having the interposer according to Claim 1.

Claim 10: The interposer according to Claim 1, wherein a diameter of each of the plurality of through holes is from 30 μm to 125 μm .

Claim 11: An interposer configured to be located between a package substrate made of resin and an IC chip, the interposer comprising:

an insulating base material, wherein a Young's modulus of the insulation base material is 55 to 440 GPa and a thickness of said insulation base material is 0.05 to 1.5 times the thickness of the package substrate; and

a plurality of through holes provided through the insulating base material,

each of said plurality of through holes having a diameter of 125 μm or less and having formed therein a through hole conductor for connecting said package substrate with the IC chip,

wherein the plurality of through holes in the insulating base material are arranged in the form of a staggered arrangement.

Claim 12: The interposer according to Claim 11, wherein a thickness of said insulation base material is at least 0.08 times the thickness of core of the package substrate.

Claim 13: The interposer according to Claim 11, wherein the size of said insulation base material is equal to or larger than projection area of an electronic component loaded on the interposer, and equal to or less than a projection area of the package substrate.

Claim 14: The interposer according to Claim 11, wherein said package substrate is a multilayer printed wiring board.

Claim 15: The interposer according to Claim 11, wherein said through hole conductor is made of metal plating.

Claim 16: The interposer according to Claim 11, wherein said through hole conductor is made of metallic paste.

Claim 17: The interposer according to Claim 11, wherein as regards the sectional shape of the through hole in the insulation base material, the diameter of an opening in at

least an end face of the through hole is equal to or larger than the diameter of the hole in the center of the through hole.

Claim 18: A multilayer printed wiring board having the interposer according to Claim 11.

Claim 19: The interposer according to Claim 11, wherein a diameter of each of the plurality of through holes is from 30 μm to 125 μm .

Claim 20: The interposer according to Claim 1, wherein a set of said plurality of through holes corresponding to either a power source electrode or ground electrode terminal of the IC chip are arranged in said grid.

Claim 21: The interposer according to Claim 20, wherein the plurality of through holes are arranged to effect substantially uniform temperature of the interposer.

Claim 22: The interposer according to Claim 1, wherein each of the plurality of through holes are arranged at substantially equal distance from each other.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.